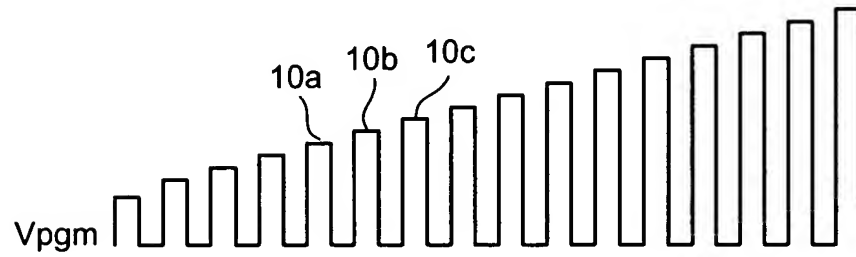


Fig. 1



of cells

Fig. 2

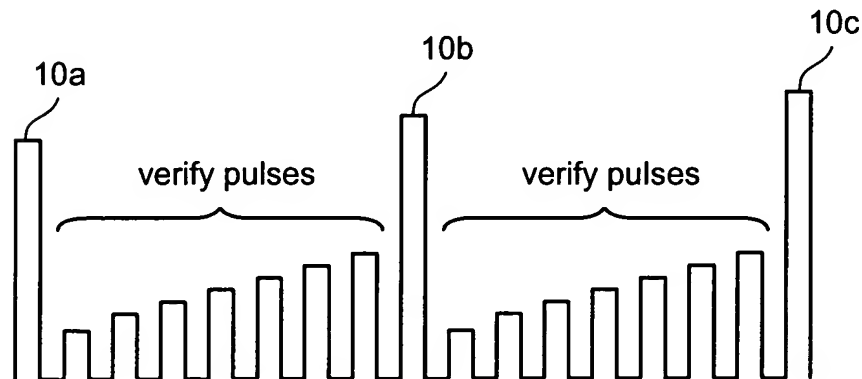
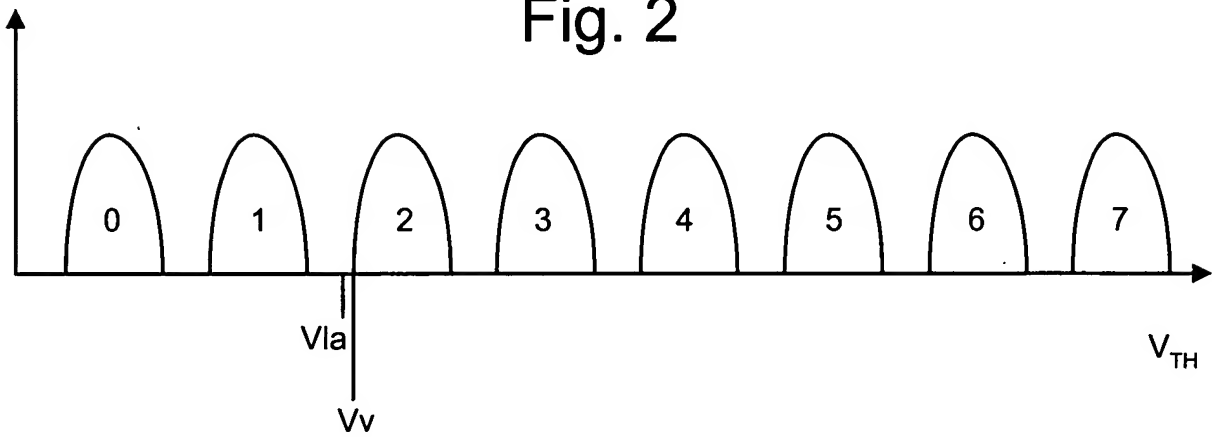


Fig. 3

Fig. 4

The diagram illustrates a memory system architecture with the following components and connections:

- Host (35)**: Connected to the **Controller (27)** via a bidirectional arrow.
- Controller (27)**: The central management unit, connected to several other blocks.
 - Connected to **Steering Gates Decoders and Drivers (21)** via a **Control/Status** line (33).
 - Connected to **Select Gates (Word Lines) Decoders and Drivers (19)** via a **Control/Status** line (31) and a **Bus** (25).
 - Connected to **Bit Line Decoder, Drivers and Sense Amplifiers (22)** via a **Control/Status** line (29).
- Steering Gates Decoders and Drivers (21)**: Connected to the **memory array (11)** via a bidirectional arrow (23).
- Select Gates (Word Lines) Decoders and Drivers (19)**: Connected to the **memory array (11)** via a bidirectional arrow (17).
- memory array (11)**: The central data storage component, connected to the **Bit Line Decoder, Drivers and Sense Amplifiers (22)** via a bidirectional arrow (15).
- Bit Line Decoder, Drivers and Sense Amplifiers (22)**: Connected to the **Controller (27)** via a **Read** line (41) and a feedback line (25).

Reference numerals in the diagram include: 27 (Controller), 35 (Host), 21 (Steering Gates Decoders and Drivers), 23 (bidirectional connection), 11 (memory array), 17 (bidirectional connection), 19 (Select Gates Decoders and Drivers), 15 (bidirectional connection), 22 (Bit Line Decoder, Drivers and Sense Amplifiers), 33 (Control/Status line), 31 (Control/Status line), 25 (Bus/Feedback line), 29 (Control/Status line), and 41 (Read line).

Fig. 6

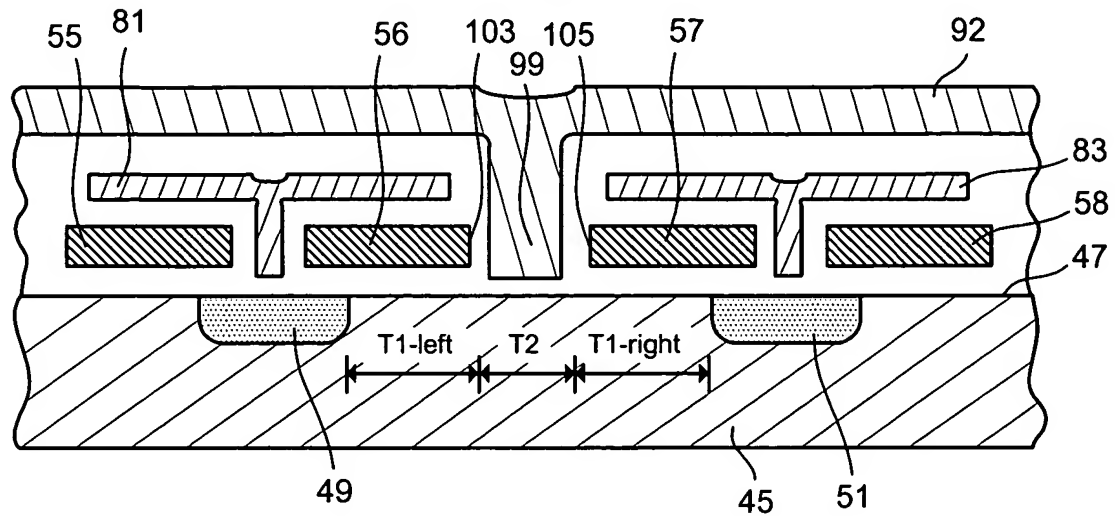


Fig. 7

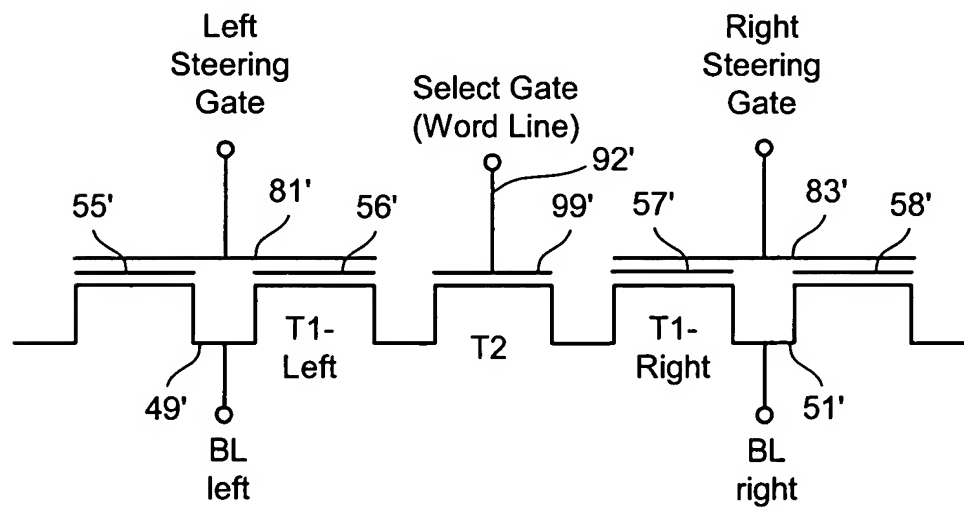


Fig. 8

FUNCTION BEING PERFORMED ON CELL	SELECT GATE (WORD LINE)	LEFT BIT LINE (BL - LEFT)	LEFT STEERING GATE	RIGHT STEERING GATE	RIGHT BIT LINE (BL-RIGHT)
(1) UNSELECTED ROW (2) ERASE (TO WORD LINE) (3) READ LEFT FLOATING GATE (4) READ RIGHT FLOATING GATE (5) PROGRAM LEFT FLOATING GATE (6) PROGRAM RIGHT FLOATING GATE (7) NO PROGRAM IN SELECTED ROW	0 V_E V_{SR} V_{SR} V_{SP} V_{SP} V_{SP}	X 5 0 1 5 0 0 5	X 0 V_M V_{BR} V_P V_{BP} X X	X 0 V_{BR} V_M V_{BP} V_P X X	X 5 1 0 0 5 0 5
(8) ERASE (TO CHANNEL) [WITH VOLTAGES OF BOTH THE p-well AND n-well EQUAL TO V_E , AND THE SUBSTRATE AT ZERO VOLTS]	V_{SE}	FLOAT	0	0	FLOAT

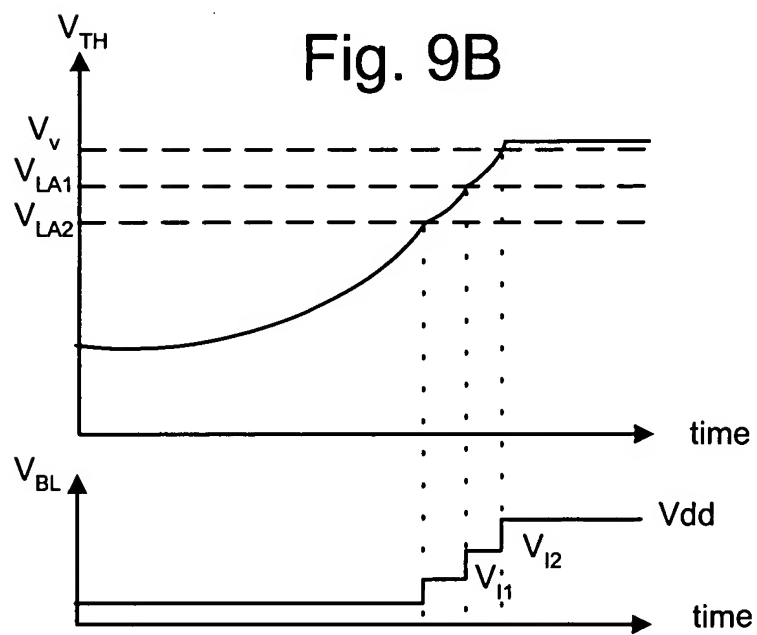
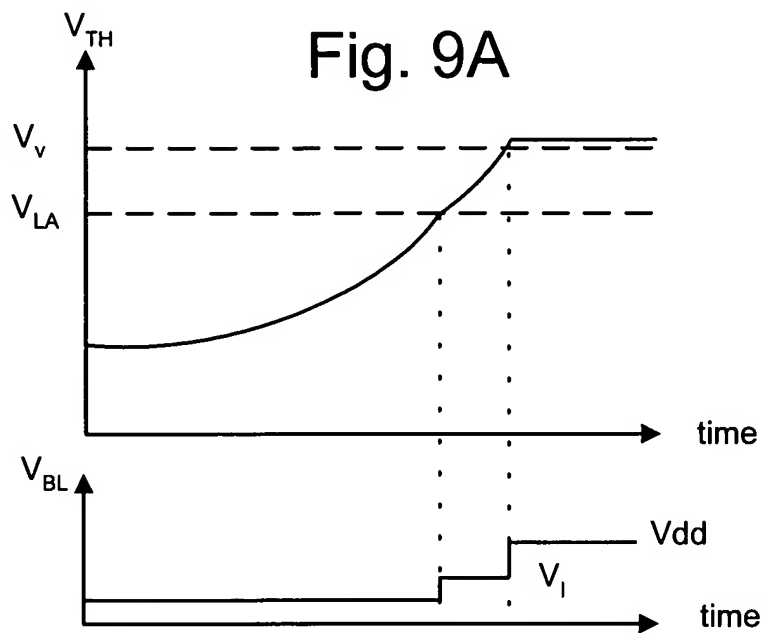
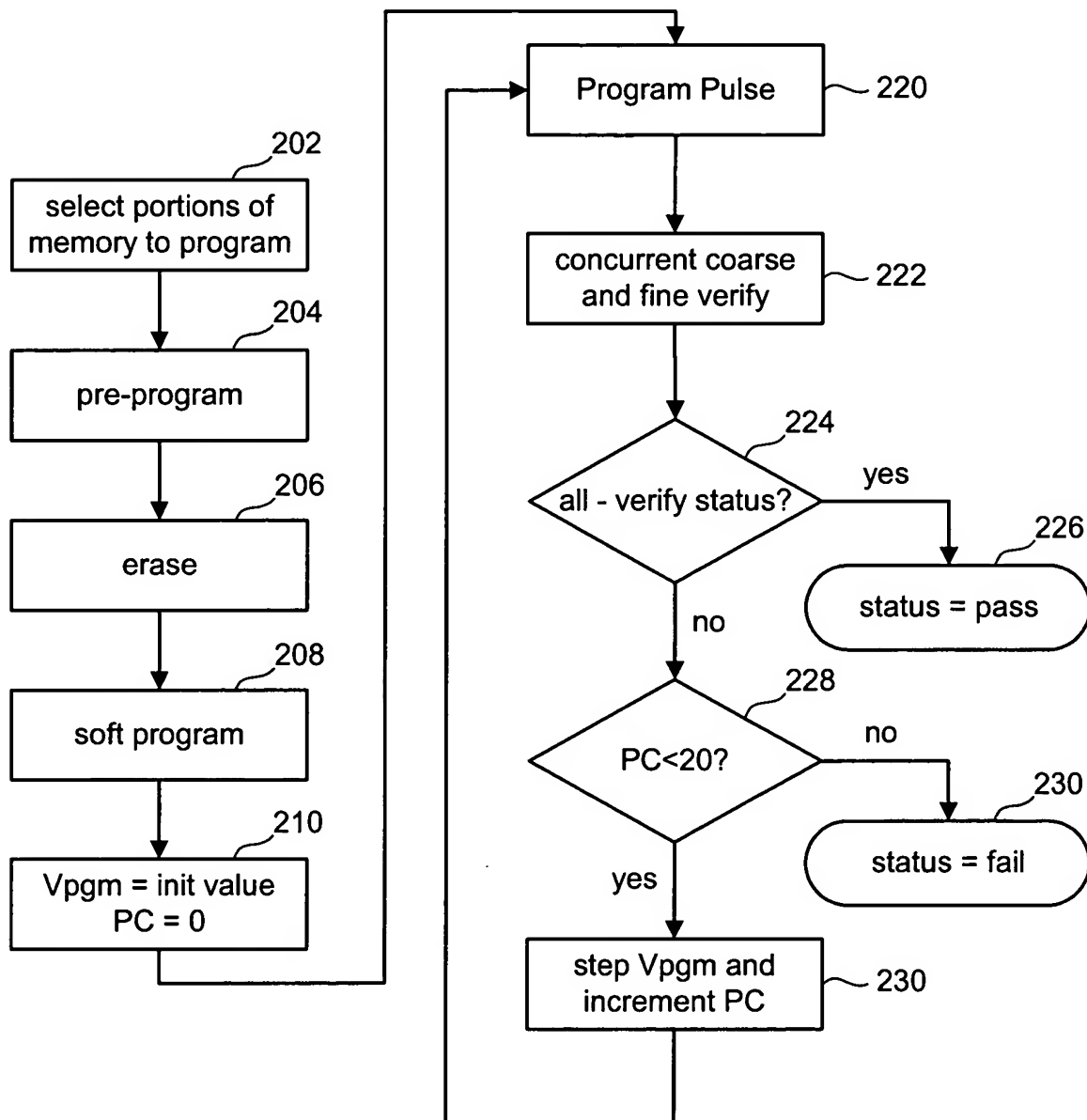


Fig. 10



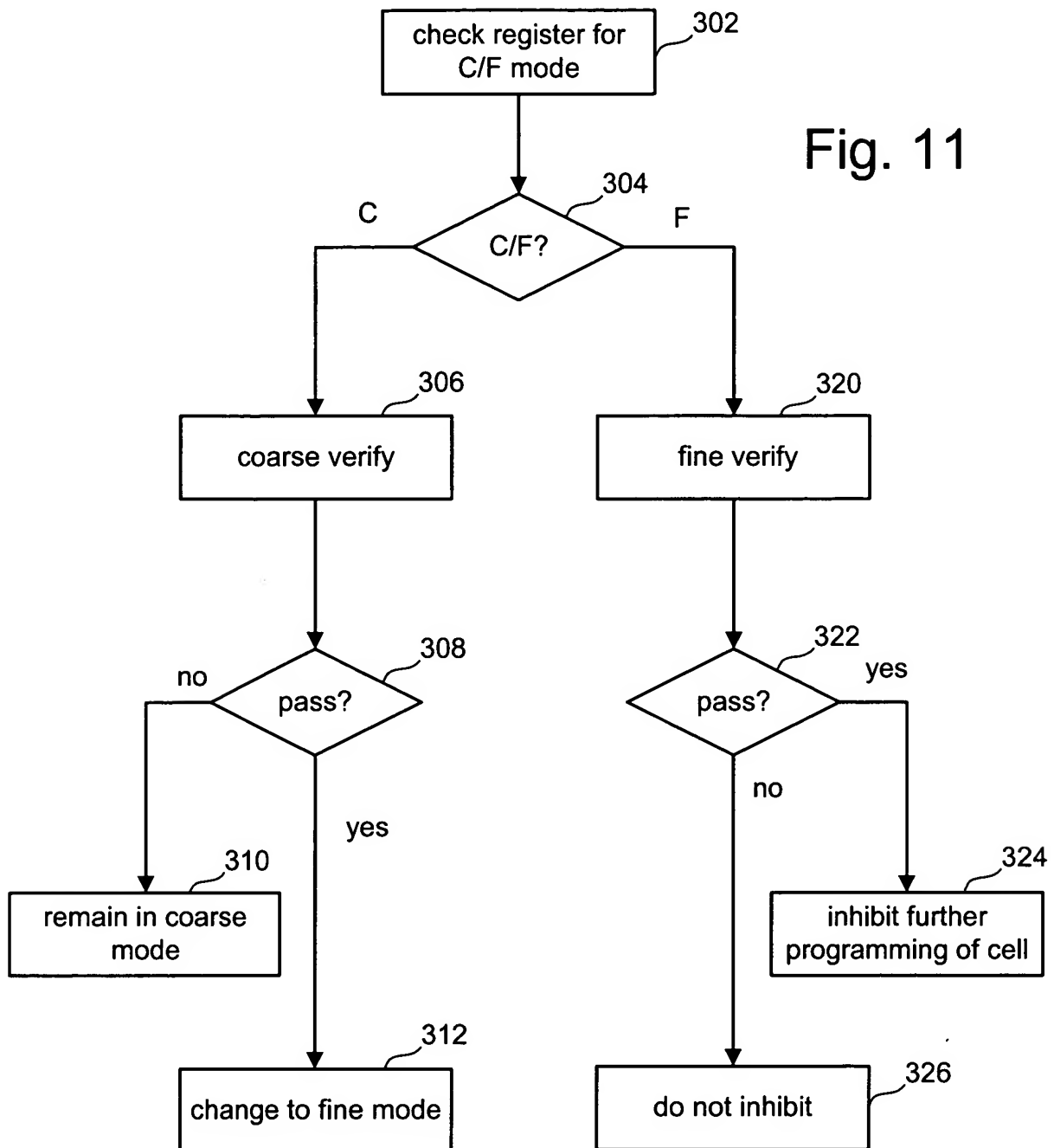


Fig. 12

A graph showing the voltage V_{bl} on the vertical axis versus time on the horizontal axis. The voltage starts at a high level, remains constant for a short duration, and then decays exponentially. A horizontal dashed line represents the reference voltage V_{ref} . The intersection of the decaying curve and the V_{ref} line is marked. A horizontal double-headed arrow labeled "compare time" spans from the start of the decay to the intersection point. A vertical dashed line at time T marks the end of the pulse.

Fig. 14

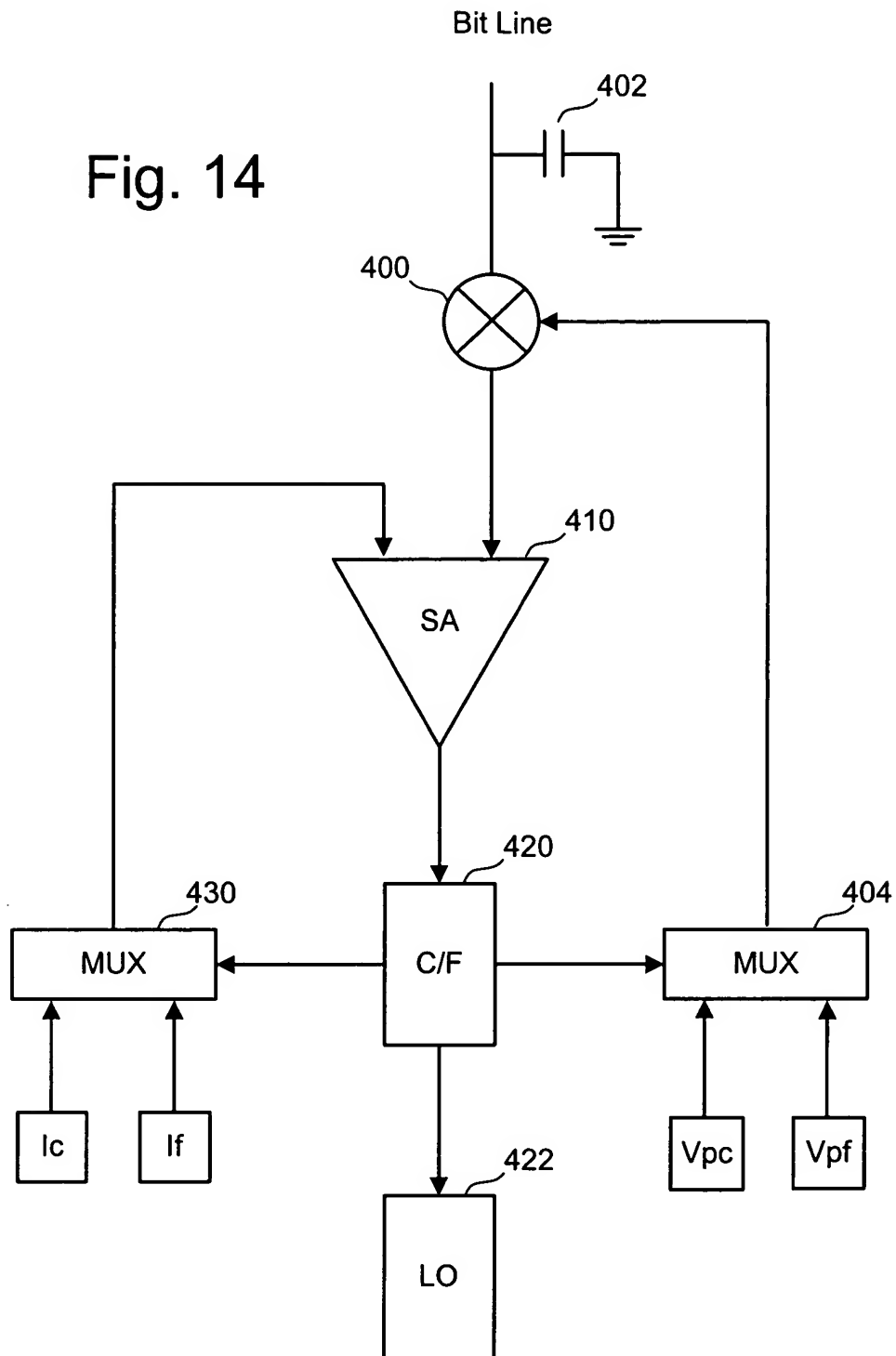


Fig. 15

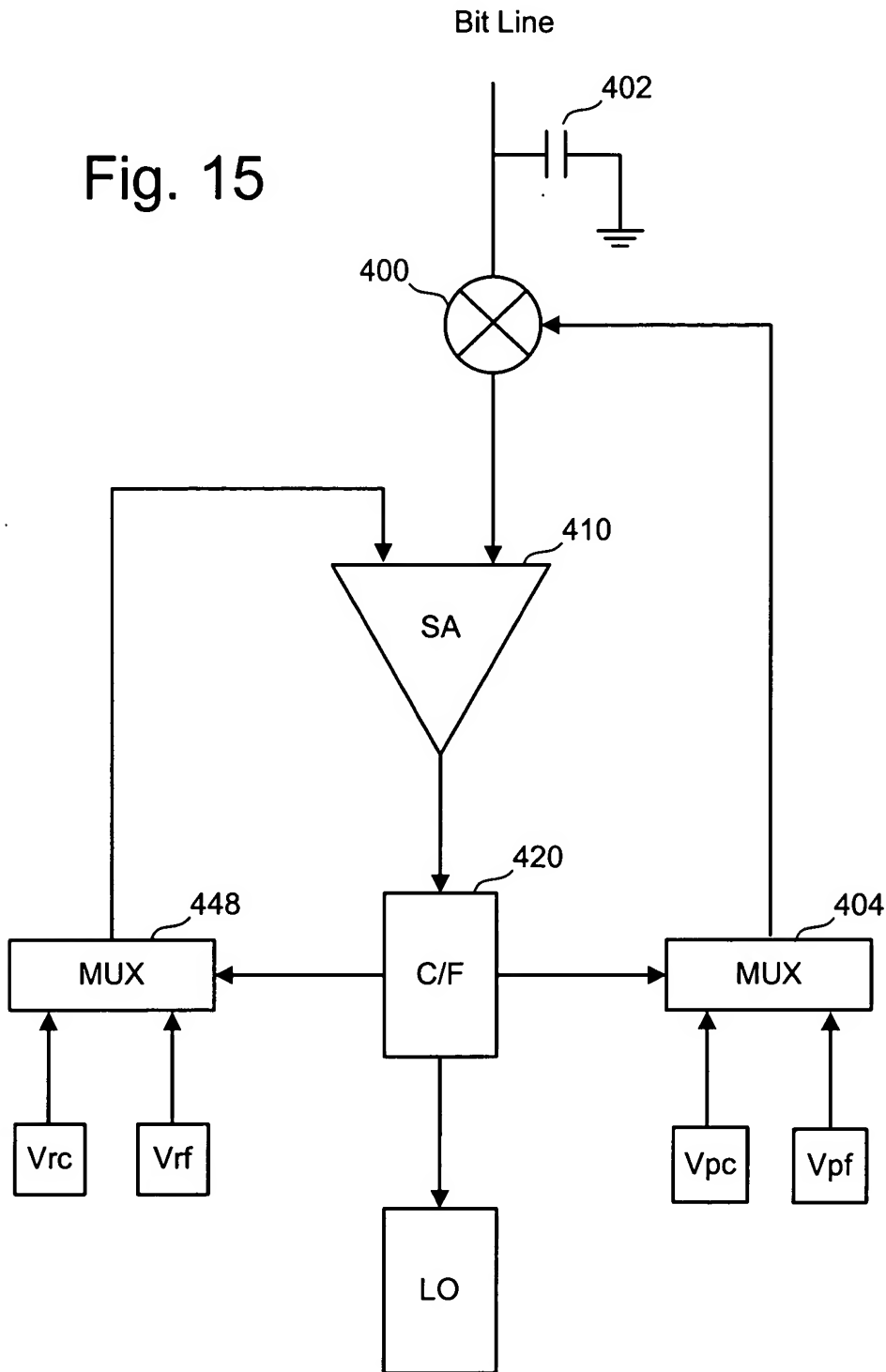


Fig. 16

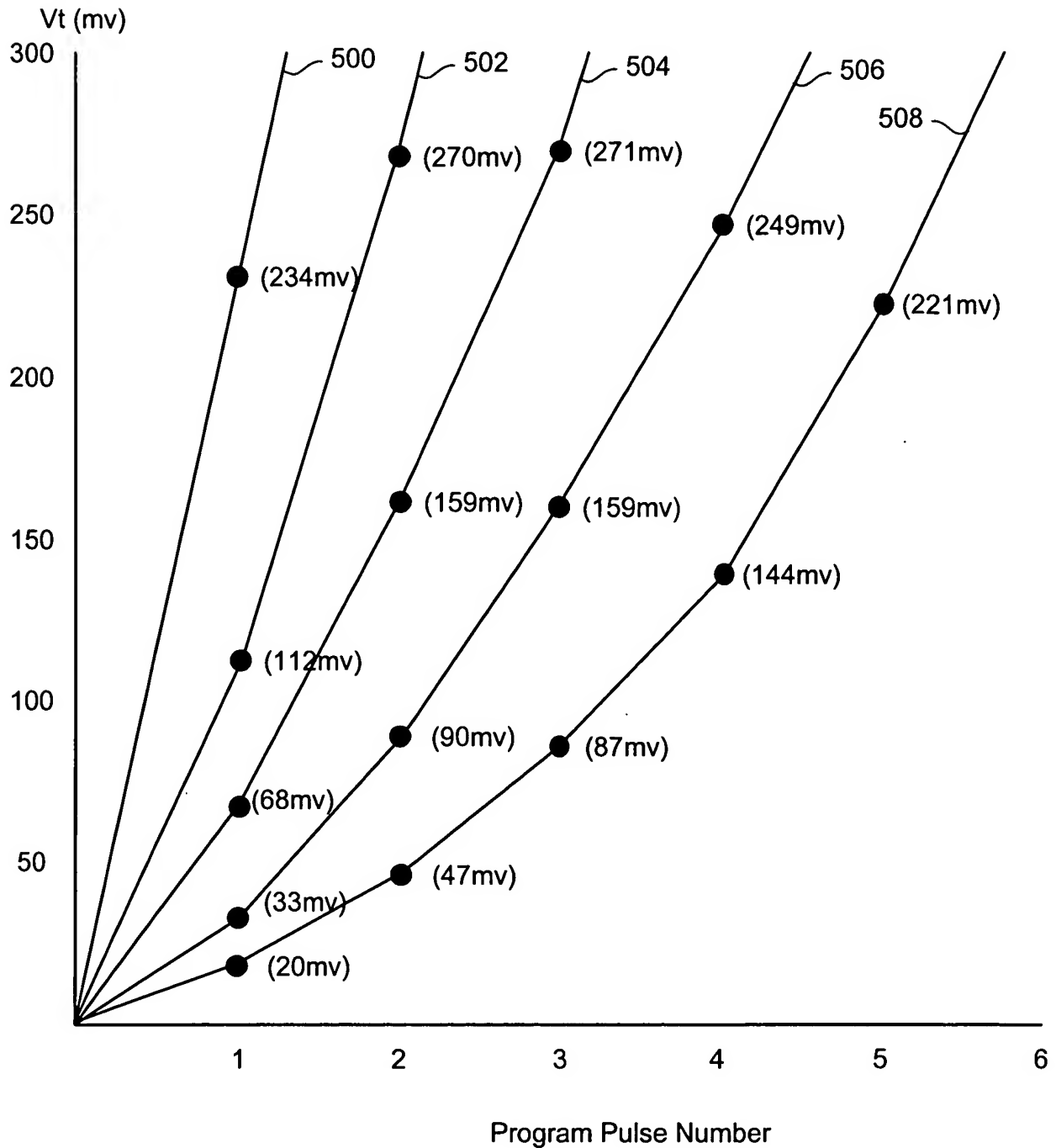


Fig. 17

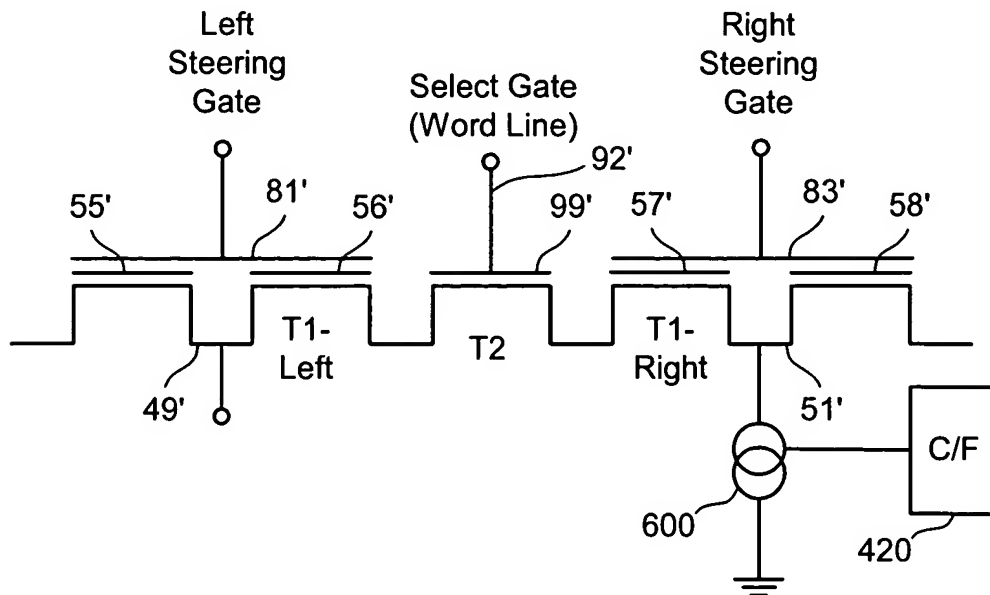


Fig. 18

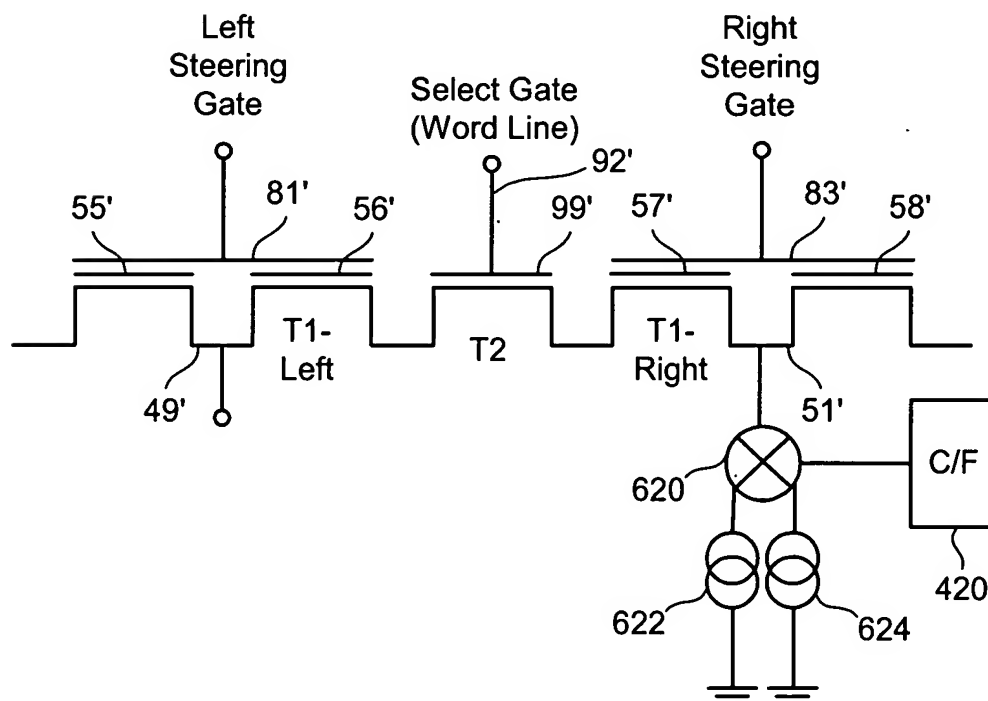


Fig. 19

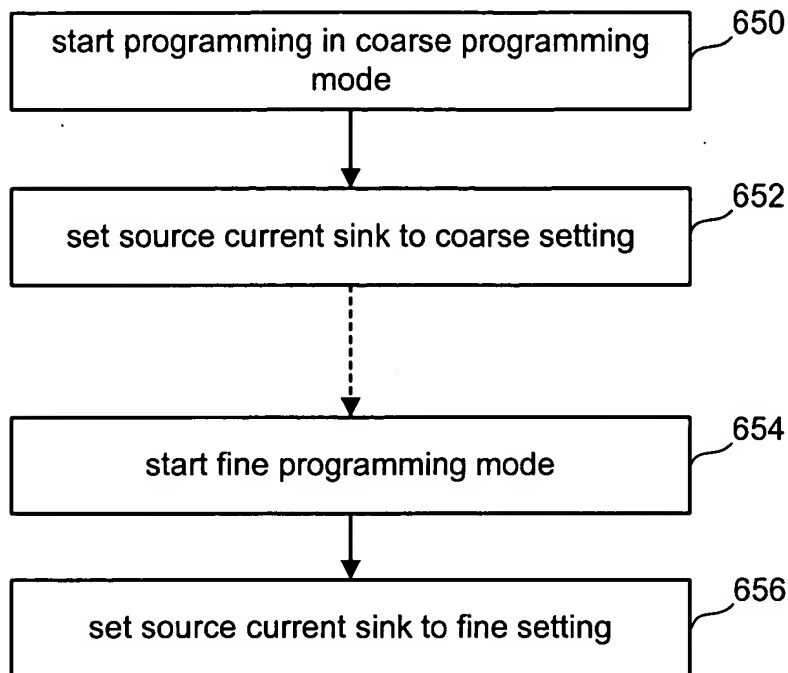
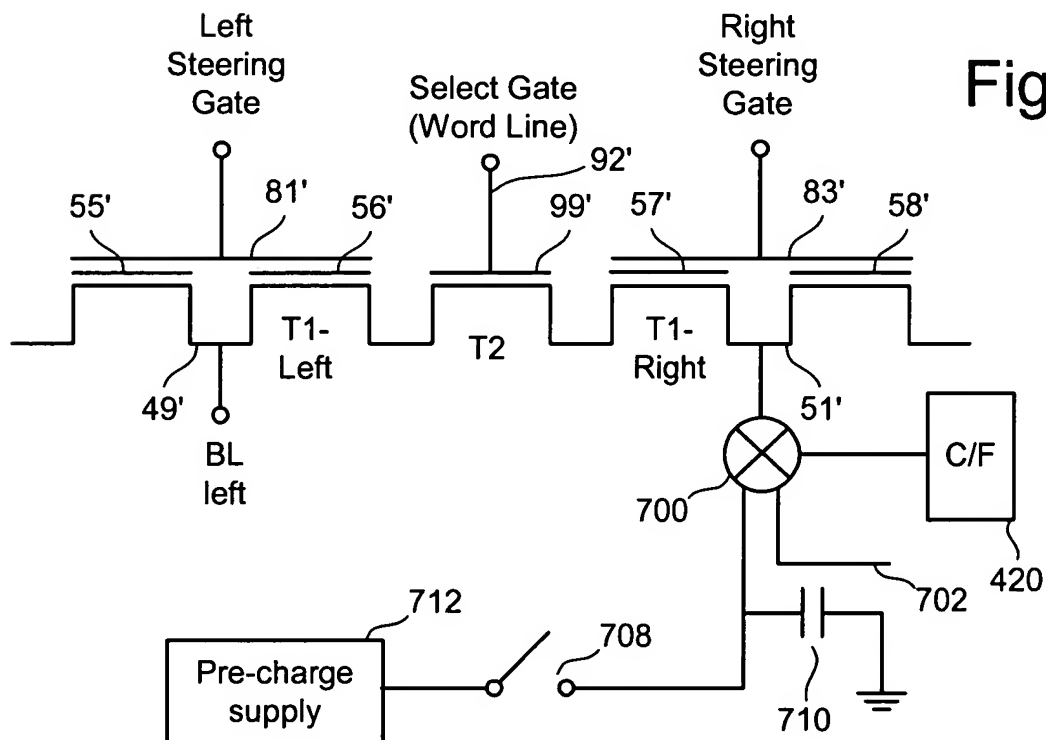


Fig. 20



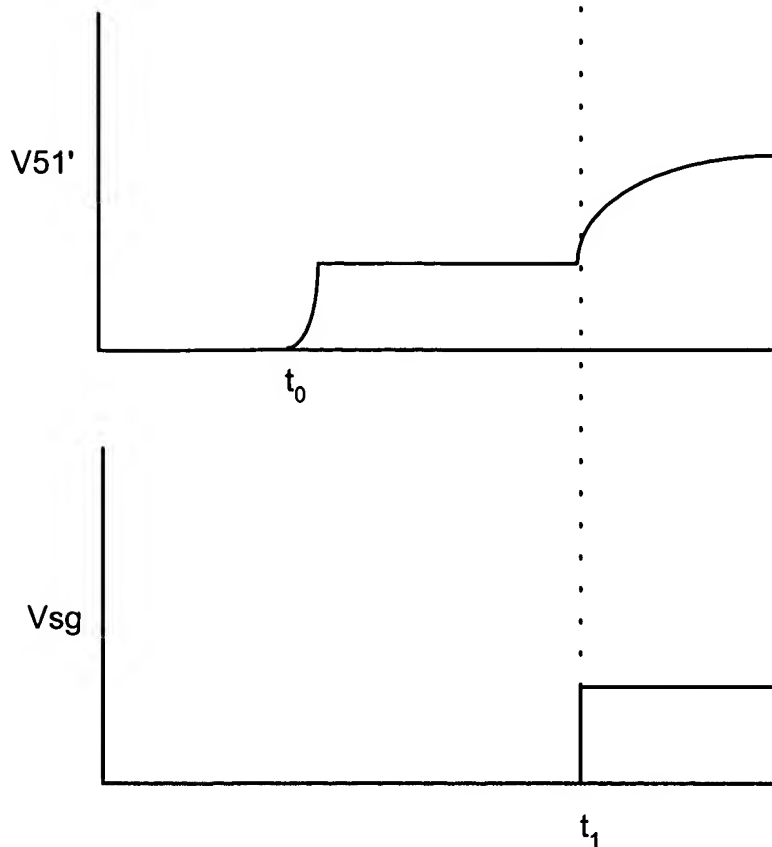


Fig. 21

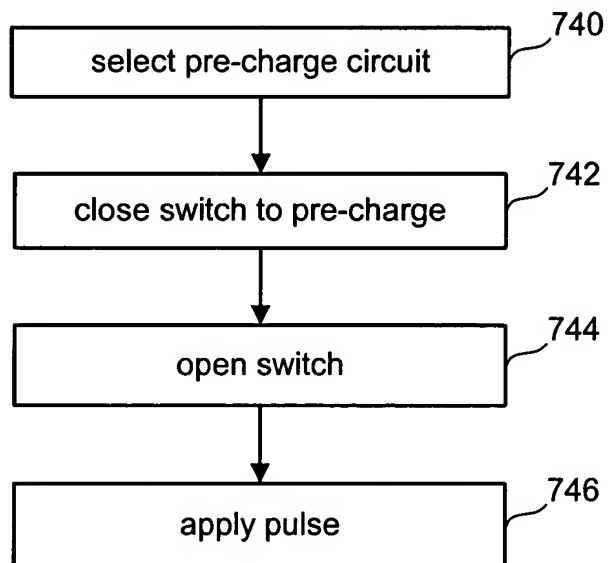


Fig. 22

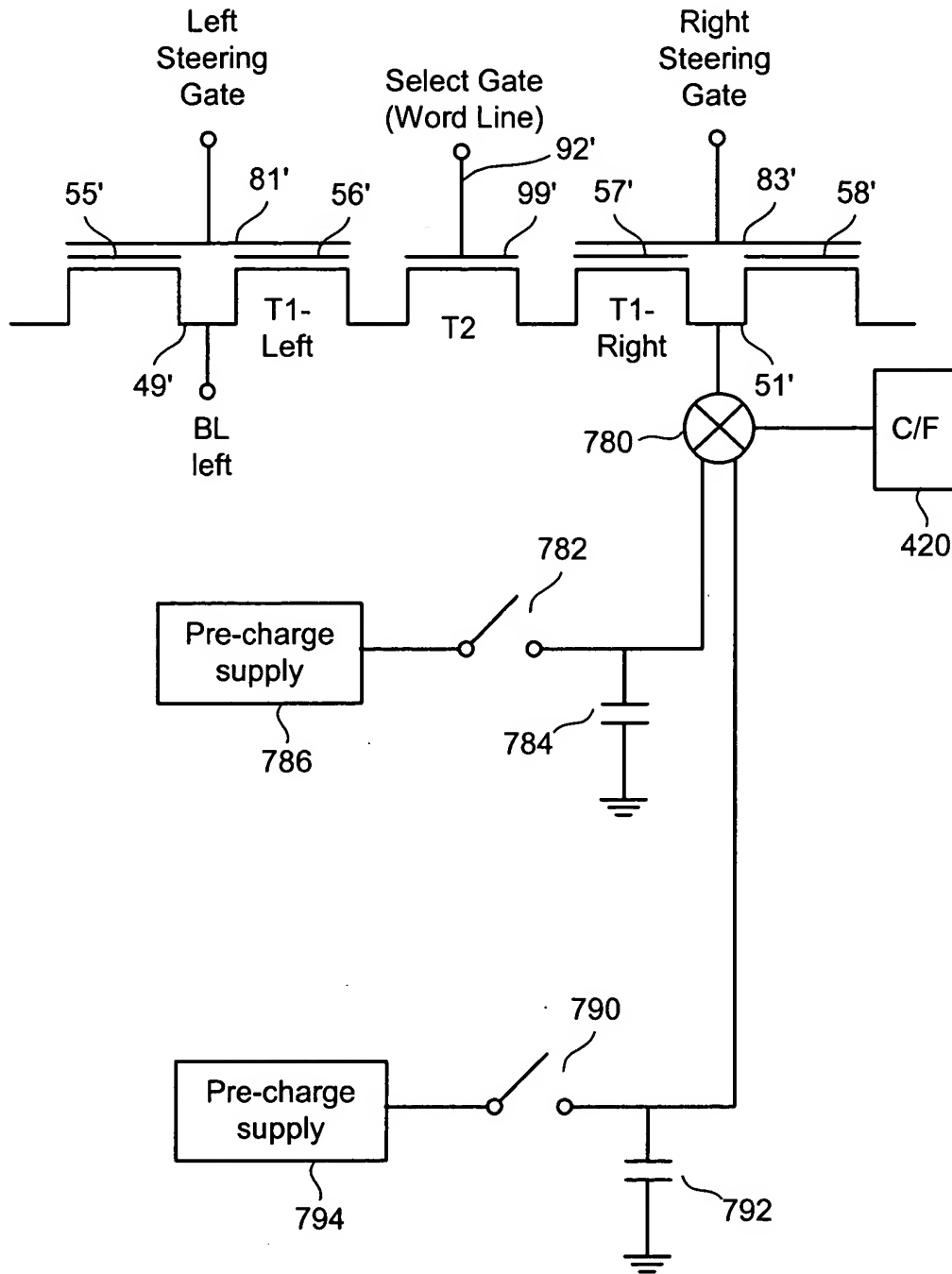


Fig. 23

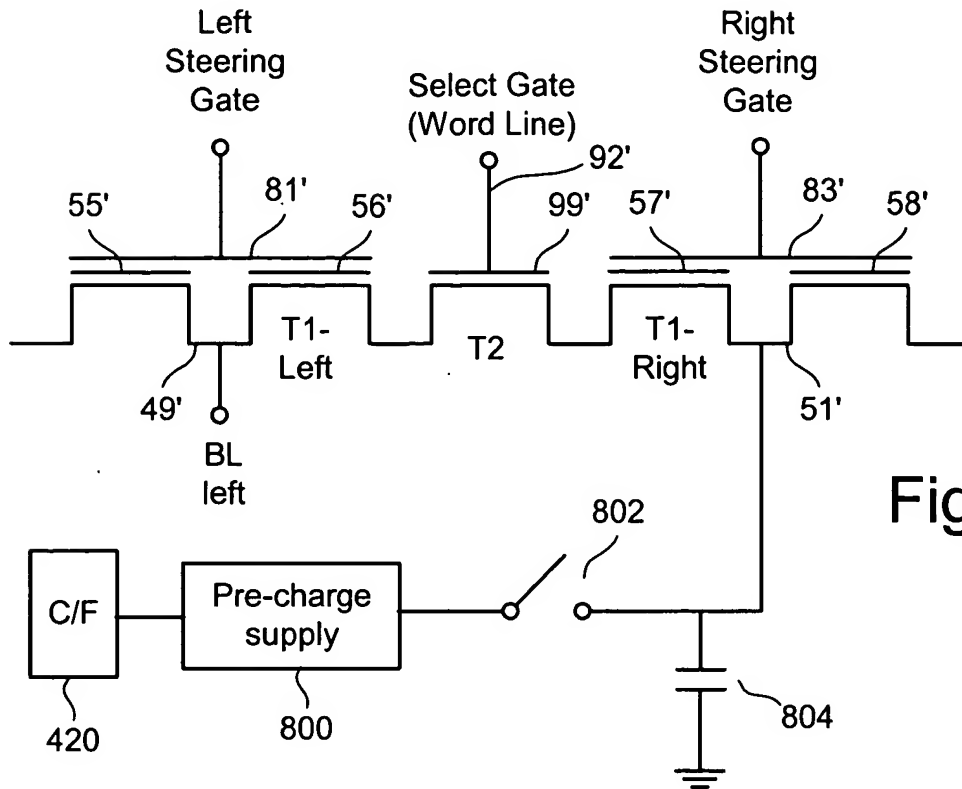


Fig. 24

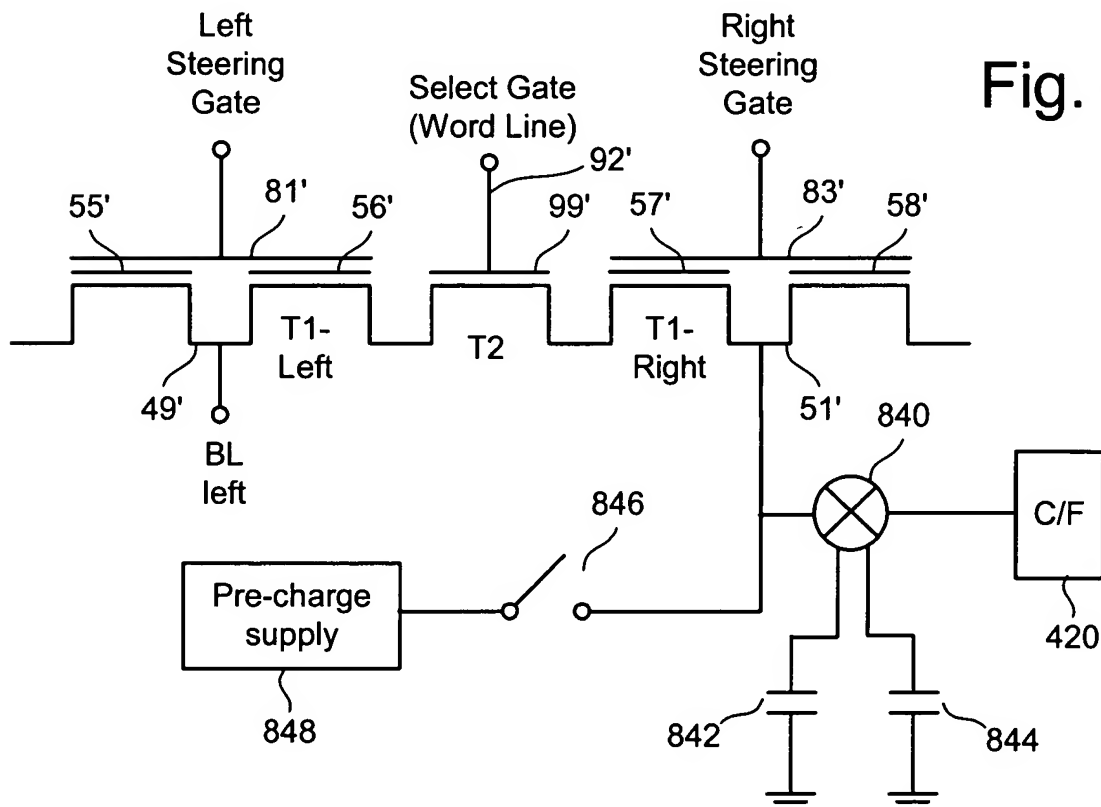


Fig. 25